

HV-EPICS Test Station Status Report

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1. Inspected and installed new SY4527 CAEN system

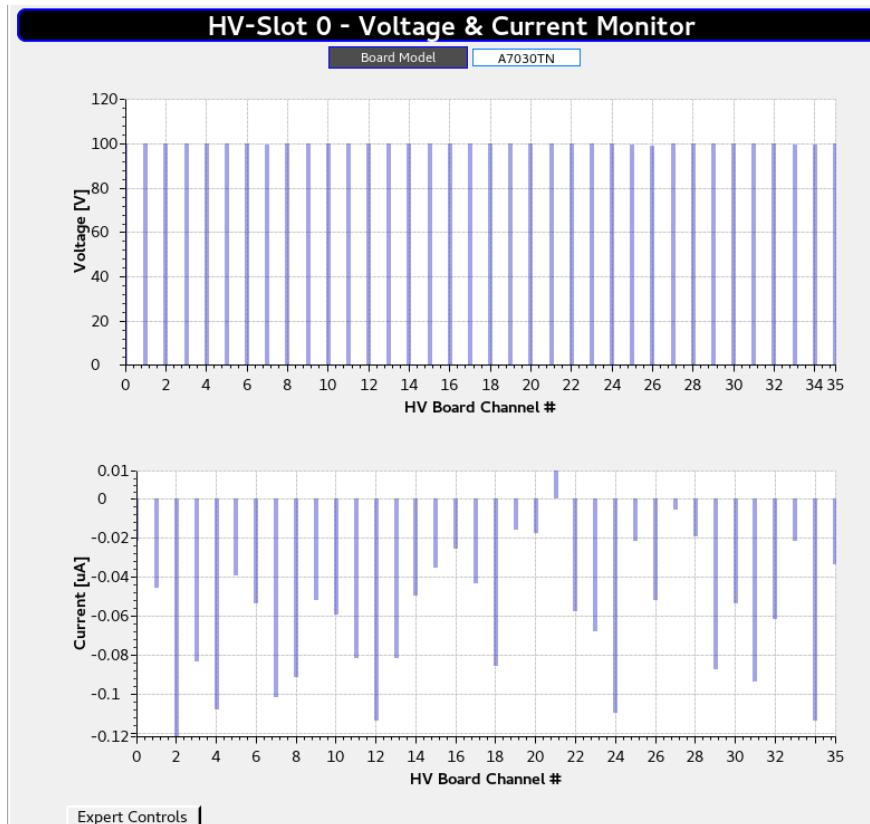
- 1.1. Received and installed seven HV modules model: A7030TN, 36 channel, 3 KV.
- 1.2. In total eleven A7030TN HV modules installed in the new SY4527 HV system.
- 1.3. Installed SY4527 system on DSG clean room.

2. Connected and configured SY4527 system to the network.

- 2.1. Verified IP (129.57.86.124) and hostname (hvcaentest2) to connect SY4527 CAEN system via Ethernet.
- 2.2. Configured and enabled EPICS Server on SY4527 CAEN systems.
- 2.3. Modified EPICS base environment variables (.cshrc file) to add new IP address of SY4527 CAEN system.
- 2.4. Used developed CSS-BOY screens and EPICS base running on dsg-b-linux1 PC to test communications and proper data transfer.

3. Started test on A7030N module located at slot 0.

- 3.1. Set channels 0-36 to 100 V and readout outputs with no issues.
- 3.2. Used same CSS-BOY screen previously developed 7435 HV module; only added the additional twelve channel in new model A7030TN HV module.



HV Voltage and Current Monitor CSS-BOY screen show bar graph for all channels in A7030TN HV module

4. Modified and developed SY4527 HV CAEN Mainframe Status CSS-BOY screen to monitor and control main parameters of SY4527 CAEN system.
 - 4.1. Added indicators and controls for HV Clock Status, Reset System Configurations and HV Fan Status.
 - 4.2. Added detail descriptions for each signal; description are based on user manual from CAEN.

SY4527 CAEN HV POWER SUPPLY - MAINFRAME STATUS

Select CAEN HV Slot v

General Status			Front Panel - Input Status			Front Panel - Output Status			Reset System Configurations		
Signal Name	Status	Description	Signal Name	Status	Description	Signal Name	Status	Description	Description	Set	Status
GEN Enable			Vsel		0 = V0 / 1 = V1	OVC		Over Current	Backplane Reset due to CPU failure	SET	
GEN Always ON			Isel		0 = I0 / 1 = I1	UNV		Under Voltage	Always set to 1	SET	
ON due to OvV		Over Voltage	Kill			OvV		Over Voltage	Backplane Reset due to Front panel reset input signal	SET	
ON due to OvC		Over Current	Interlock			CHON		Channel ON	Always set to 1	SET	
ON due to UnV		Under Voltage	Remote Enable			Bit 4 Don't care			Always set to 1	SET	
ON due to TRIP			Local Enable			Bit 5 Don't care			Always set to 1	SET	
Bit 6 Don't care			TTL/NIM		0 = TTL / 1 = NIM	Bit 6 Don't care			Always set to 0	SET	
Bit 7 Don't care			Bit 7 Don't care			Bit 7 Don't care			Always set to 0	SET	
Enable MASK			Bit 8 Don't care			Bit 8 Don't care			Always set to 0	SET	
Always ON MASK			Bit 9 Don't care			Bit 9 Don't care			Always set to 0	SET	
ON due to OvV		Over Voltage MASK	Bit 10 Don't care			Bit 10 Don't care			Always set to 0	SET	
ON due to OvC		Over Current MASK	Bit 11 Don't care			Bit 11 Don't care			Always set to 0	SET	
ON due to UnV		Under Voltage MASK	Bit 12 Don't care			Bit 12 Don't care			Always set to 0	SET	
ON due to TRIP MASK			Bit 13 Don't care			Bit 13 Don't care			Always set to 0	SET	
Bit 14 Don't care			Bit 14 Don't care			Bit 14 Don't care			Always set to 0	SET	
Bit 15 Don't care			Bit 15 Don't care			Bit 15 Don't care			Always set to 0	SET	

HV Power Supply Module Status		Primary Power Supply Status			Network Status			HV System Status		
Description	Status	Description	Set	Readback	Description	Set	Readback	Feature	Readback	Description
Returns string with power supply module status Format : ACstatus : Primary : Add 0 : Add 1 : Add 2	1:1:A4532:0:0	Power Supply Current	1.44A:1.72A:0:	1.44A:1.72A:0:	IP ADDRESS	129.57.86.124	129.57.86.124	System Mod. Name	SY4527	System model name
AC status = -1 -> FAIL AC status = 1 -> GOOD Primary = -1 -> Module FAIL Primary = 1 -> Module GOOD Add X = -1 -> Addon Sup. FAIL Add X = 0 -> Addon Sup. NOT PRESENT Add X = 1 -> Addon Sup. GOOD		Power Supply Voltage	0	0	IP NET MASK	255.255.255.0	255.255.255.0	System firmware Ver.	2.0.2 - 0.08	Downloaded firmware
					IP GATEWAY	129.57.86.1	129.57.86.1	Login Session	admin:admin:TCP/IP:Tue Jun 18 20_40_54	
								System Symbolic Name	SystemOne	
								CPU Load	00: CPU1 : 00: CPU2 : 00: CPU3	CPU Average Used
									00:52:00:54:00:50	
								Memory Status	TOTAL MEMORY : USED MEMORY : FREE MEMORY : BUFFER MEMORY	
									1968308:1877620: 5212: 3116	

HV Clock Status		HV Fan Status							
Description	Set	Description		Status					
FAIL = -1 50 HZ = 0 60 HZ = 1 400 HZ = 2	1	FAIL = -1	GOOD = 1	Fan#1	Fan#2	Fan#3	Fan#4	Fan#5	Fan#6
MASTER = 1 SLAVE = 0 FAIL = -1 NOT PRESENT = 0 GOOD = 1	1:0			1:2395:1:2252:1:2324:1:2395:1:2217:1:23					

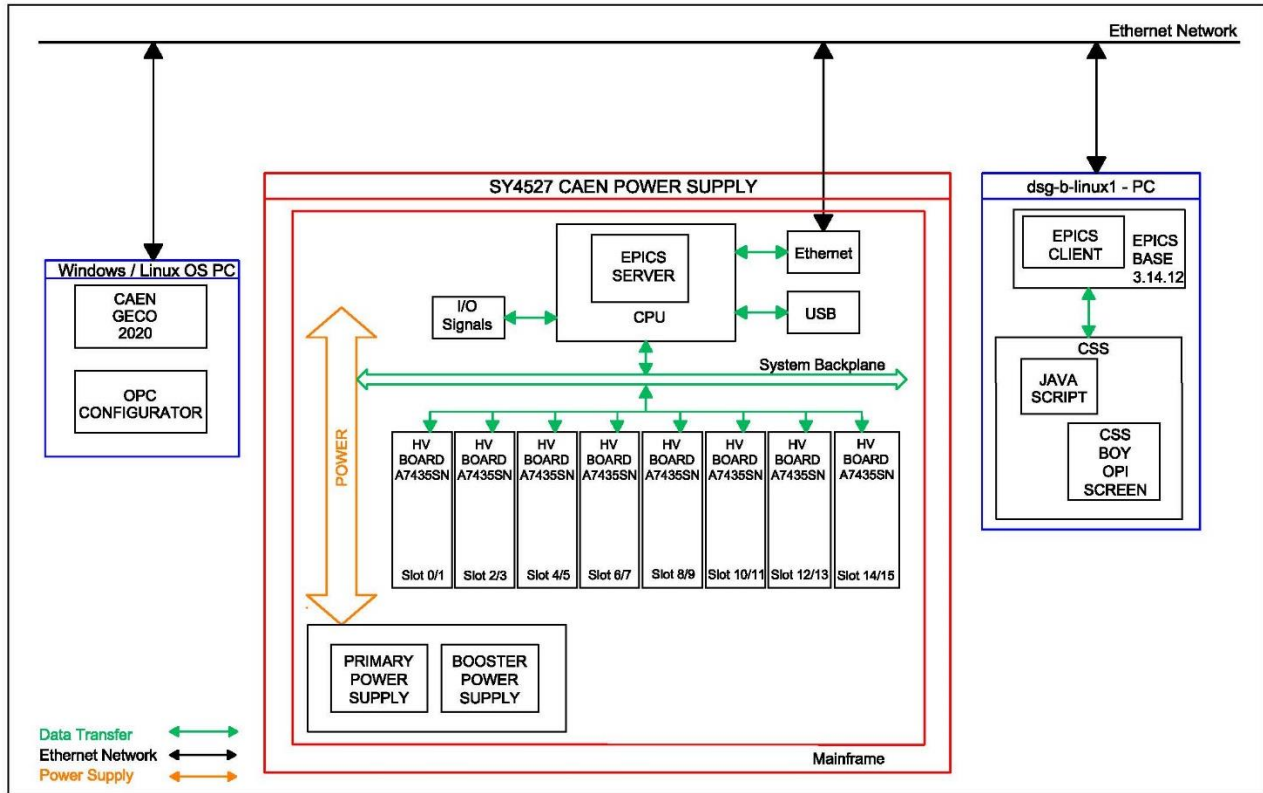
campero

SY4527 CAEN System Mainframe Status CSS-BOY screen

5. Developing of EPICS database to control and monitor HV CAEN SY4527 power supply in progress.

6. Generated diagram to show HV-EPICS test station setup.

6.1. Diagram shows main hardware and software components needed for HV-EPICS test station.



HV-EPICS test station setup diagram